



- [c5] The memory device according to claim 1 wherein a first access port and a second access port are provided; said first access port comprising said first wordline decoder and said second access port comprising said second wordline decoder; a terminal to provide a first select signal to enable an access through said first port and a terminal to provide a second port select signal to enable an access through said second port; said contention circuit providing an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if the port select signal provided to said first access port is activated and the port select signal provided to said second access port is deactivated.
- [c6] The memory device according to claim 5 wherein said contention circuit provides an address of a wordline of which the memory cells are to be refreshed to said row decoder of said first access port, if the port select signals provided to said first and second access ports are both activated, and wherein said contention circuit issues a wait signal to delay an externally requested access to a memory cell through said first access port during said refresh performed through said first access port.
- [c7] The memory device according to claim 5 or 6 wherein said contention circuit is designed to perform a wait cycle for an externally requested access for one of said ports, if the first and the second port select signals are activated.
- [c8] The memory device according to any of claims 1 to 7, wherein the memory cells each comprise a storage device having a first and a second terminal, a first access transistor connected to said first terminal and a second access transistor connected to said second terminal, said first access transistor connected to one of the multitude of said first wordlines and first bitlines, said second access transistor connected to one of the multitude of second wordlines and second bitlines.
- [c9] A method of operating a memory device wherein said memory device has first and second access ports, memory cells being arranged in a multitude of rows, each row being accessible through said first and said second ports, and first and second row decoders decoding one of said rows in response to a respective

row address, wherein a refresh is performed on the memory cells of one of said rows by enabling said row through the first row decoder while another row is accessed in response to an externally requested access through the second row decoder.

[c10] The method according to claim 9 wherein a wait cycle for an externally requested access is issued for said one port of said first row decoder when the first and the second access ports each receive an externally requested access.

[c11] The method according to claim 9 further comprising the step of counting the row address of rows to be refreshed and suppressing a refresh of the memory cells of a row when a row address of an externally requested access and the row address of said row to be refreshed match each other.